METHODS TO CONTROL THE DROOP WHEN POWERING DUAL MODE PROCESSORS AND ASSOCIATED CIRCUITS

ABSTRACT

A DC/DC converter 100 has a DAC 40 that receives a code associated with desired processor operating voltage and sets the reference voltage on its output 41. The reference voltage (V_{DAC}) is boosted by the buffer amplifier 42 to center the droop along the median load. A sensed current signal I_{CS} 22 is proportional to the load current I_o 24 and can be either inductor current, or switch current, or diode (or synchronous switch) current. In all cases it is scaled down by the factor of gain G_c. A droop control feedback circuit includes an error amplifier 50. It has two inputs. In one embodiment the gain of the converter is by a signal inversely proportional to the processor clock frequency $F_{CPU\,max}$ and transformed to the current I_{DROOP} 32 that creates the voltage drop across the resistor R1. The other input is coupled to the buffer amplifier output. As a result, the output voltage of the converter 50 is inversely proportionally to the load current and is invariant to the processor clock frequency changes associated with the processor mode switchover. Other embodiments modify the gain of the error amplifier, or offset the gain and hold the amount of droop constant.